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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,654	09/18/2003	David Jia Chen	ROC920030233US1	8565

23334 7590 07/01/2005

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EXAMINER	
NGUYEN, LINH M	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,654	CHEN ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

RCE acknowledgement/ Prosecution reopened

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after a final office action or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 05/26/2005 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claims, 1, 9, 10 and 11, the recitation "minimum channel length" renders the claims indefinite since the term "minimum" in the claims is a relative term which renders the claim indefinite. The term "minimum" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claims 2-8 and 12-14 are rejected under 35 U.S.C. 112, second paragraph because of the dependency on claims 1 and 11.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al. (U.S. Patent No. 5,602,798) in view of Shimotsusa et al. (U.S. Pub. No. 2004/0046211) and in view of Harrington, III (U.S. Patent No. 4,943,537).

With respect to claim 1, 9 and 10, as best understood, Sato et al. discloses, in Fig. 14A, a circuit arrangement comprising a) an input signal [ID1] to be delayed and b) a series of at least two delay stage [60a-60n], wherein each of the delay stages includes a stack of transistors [P3, N1] with a first group of a first conductivity type [p-channel] and a second group of transistors of a second conductivity type [n-channel], wherein a gate of each of the transistors in each of the delay stages are electrically coupled together to form an input in each of the delay stages, wherein a source of a top transistor in the stack is coupled to a first reference voltage [Vcc], wherein a source of a bottom transistor in the stack is coupled to a second reference voltage [ground], and wherein a drain of the top transistor is electrically coupled to a drain of the bottom transistor in the stage so as to form an output of the stage; wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.

Sato fails to explicitly disclose the use of uniform minimum channel length transistors provides uniform tolerance variations across a circuit.

Shimotsusa et al. discloses, in page 16, paragraph [0239], an array of transistors with uniform channel lengths which high reliability can be obtained.

To configure the circuit of Sato et al. with uniform channel length transistors as taught by Shimotsusa et al. so that the transistors can be manufactured without any diffusion in their threshold values thus provides high reliability across the circuit would have been obvious to one of ordinary skill in the art at the time of the invention since Shimotsusa et al. teaches that such configuration would facilitate high yield and high reliability *(see Shimotsusa et al., page 16, paragraph [0239])*.

Harrington, III, discloses, in column 4, lines 4-9, that the use of minimum channel length confers several advantages regarding drive capability, on-state series resistance and switching speed.

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure the combined circuit of Sato et al. and Shimotsusa et al. with *minimum* channel length transistors as taught by Harrington, III, for increasing drive capability of the device, decreasing the on-state series resistance and also increasing the switching speed of logic circuits since such circuit arrangement for the stated purpose has been a well known practice as evidenced by the teachings of Harrington, III *(see Harrington., col. 4, lines 4-9)*.

With respect to claim 2, the combined teaching of Sato et al., Shimotsusa et al. and Harrington, III discloses that each stack of transistors includes additional transistors electrically coupled with the top transistor [P3] and the bottom transistor [N1]; wherein a drain of a first

additional transistor [P2] is electrically coupled to a source of the top transistor, a drain of the last additional transistor [N2] is connected to a source of the bottom transistor, and wherein a drain of each of zero or more remaining additional transistors is electrically coupled to a source of an adjacent transistor within the remaining additional transistors so as to form a totem pole configuration for the stack, as called for in claim 2;

With respect to claims 3-6, the combined teaching of Sato et al., Shimotsusa et al. and Harrington, III discloses that delay elements comprised both n-channel FET and p-channel FET.

With respect to claims 7 and 8, the combined teaching of Sato et al., Shimotsusa et al. and Harrington, III discloses that the input signal to be delayed is a clock signal.

With respect to claim 11, as best understood, Sato et al. discloses, in Fig. 14A, a delay circuit comprising at least one stack of transistors, each of the at least one stack of transistors comprising a first transistor [P3] with a source electrically coupled to a first reference voltage [Vcc]; a last transistor [N1] with a source electrically coupled to a second reference voltage [Ground]; a totem pole of at least two transistors, the totem pole including: a top transistor [P2] with a source electrically coupled to a drain of the first transistor; a bottom transistor [N2] with a source electrically coupled to a drain of the last transistor and at least two transistors, wherein the transistors complete the totem pole arrangement, wherein a drain of each of the transistors is electrically coupled to a source of an adjacent transistor within the transistors relative to the each of the transistors, and wherein each of the transistors within the totem pole comprise a channel length transistor with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type; the use of uniform minimum channel length transistors provides uniform tolerance variations across the delay circuit; an input electrically

coupled to each gate within the totem pole; and an output electrically coupled to connection between one source and one drain of two transistors within the totem pole; wherein when the input is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive: and wherein when the input to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.

Sato fails to explicitly disclose the use of uniform minimum channel length transistors provides uniform tolerance variations across the delay circuit.

Shimotsusa et al. discloses, in page 16, paragraph [0239], an array of transistors with uniform channel lengths which high reliability can be obtained.

To configure the circuit of Sato et al. with uniform channel length transistors as taught by Shimotsusa et al. so that the transistors can be manufactured without any diffusion in their threshold values thus provides high reliability across the circuit would have been obvious to one of ordinary skill in the art at the time of the invention since Shimotsusa et al. teaches that such configuration would facilitate high yield and high reliability *(see Shimotsusa et al., page 16, paragraph [0239])*.

Harrington, III, discloses, in column 4, lines 4-9, that the use of minimum channel length confers several advantages regarding drive capability, on-state series resistance and switching speed.

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure the combined circuit of Sato et al. and Shimotsusa et al. with *minimum* channel length transistors as taught by Harrington, III, for increasing drive capability of the device,

decreasing the on-state series resistance and also increasing the switching speed of logic circuits since such circuit arrangement for the stated purpose has been a well known practice as evidenced by the teachings of Harrington, III *(see Harrington., col. 4, lines 4-9).*

With respect to claims 12-14, the combined teaching of Sato et al., Shimotsusa et al. and Harrington, III discloses that delay elements comprised both n-channel FET and p-channel FET.

Remarks and Conclusion

6. Applicants' arguments with respect to claims 1 and 9-11 filed on 05/26/2005 have been considered but are moot in view of the new ground(s) of rejection due to newly discovered prior arts to Shimotsusa et al. and Harrington, III.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Fri, Monday - Thursday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LINH MY NGUYEN
PRIMARY EXAMINER